What is claimed is:

1. A packaging assembly comprising:

a substrate defined by a first surface and a second surface opposing to the first surface;

a plurality of chip-site lands disposed on the first surface;

a plurality of first solder balls connected to the chip-site lands;

a plurality of second solder balls connected to the first solder balls including solder materials having higher melting temperatures than the first solder balls;

a semiconductor chip having a plurality of bonding pads connected to the second solder balls on a surface of the semiconductor chip; and

an underfill resin disposed around the first and second solder balls.

2. The packaging assembly of claim 1, wherein the first solder balls include at least one material selected from the group consisting of Sn-Bi, Sn-Bi-Ag, Sn-Zn, Sn-Zn-Bi, Sn-Bi-In, Bi-In, Sn-In, Bi-Pd, In-Ag, and Sn-Pb.

3. The packaging assembly of claim 1,wherein the second solder balls include at least one material selected from

the group consisting of Sn-Ag, An-Ag-Cu, Sn-Pb, and Sn-Zn.

4. The packaging assembly of claim 1, wherein a protective film containing an organic synthetic resin is disposed on the surface of the semiconductor chip.

5. The packaging assembly of claim 1, wherein a low dielectric constant film is stacked on the surface of the semiconductor chip.

6. The packaging assembly of claim 5, wherein an effective dielectric constant of the low dielectric constant film is equal to or less than 3.5.

7. The packaging assembly of claim 1, further comprising:

a circuit element merged in the semiconductor chip; and

a multilevel-interconnection disposed on the surface of the semiconductor chip having:

a plurality of insulating films; and

a plurality of metallic interconnections alternatively stacked with the insulating film, wherein the coherence strength of the stacked structure to the semiconductor chip is equal to or less than 15 J/m^2.

8. The packaging assembly of claim 7, wherein the insulating films are made from low dielectric constant films.

9. The packaging assembly of claim 1, further comprising:

a plurality of second chip-site lands disposed on the first surface;

a plurality of third solder balls connected to the second chip-site lands;

a plurality of fourth solder balls connected to the third solder balls including solder materials having higher melting temperatures than the third solder balls;

a second semiconductor chip having a plurality of a second bonding pads connected to the fourth solder balls on a surface of the second semiconductor chip; and

an underfill resin disposed around the third and fourth solder balls.

10. The packaging assembly of claim 9, wherein the third solder balls include at least one material selected from a group consisting of Sn-Bi, Sn-Bi-Ag, Sn-Zn, Sn-Zn-Bi, Sn-Bi-In, Bi-In, Sn-In, Bi-Pd, In-Ag, and Sn-Pb.

11. The packaging assembly of claim 9,wherein the fourth solder balls include at least one material selected from a group consisting of Sn-Ag, An-Ag-Cu, Sn-Pb, and Sn-Zn.

12. The packaging assembly of claim 9, wherein a low dielectric constant film is stacked on the surface of the second semiconductor chip.

13. The packaging assembly of claim 12, wherein an effective dielectric constant of the low dielectric constant film is equal to or less than 3.5.

14. The packaging assembly of claim 9, further comprising:

a second circuit element merged in the second semiconductor chip; and

a second multilevel-interconnection disposed on the second semiconductor chip having:

a plurality of insulating films; and

a plurality of metallic interconnections alternatively stacked with the insulating film, wherein the coherence strength of the second multilevel-interconnection to the second semiconductor chip is equal to or less than 15 J/m^2.

15. The packaging assembly of claim 14, wherein the insulating films are made from low dielectric constant films.

16. A method of assembling a packaging assembly comprising:

preparing a substrate having a plurality of chip-site lands disposed on the first surface of a substrate;

disposing a plurality of first solder balls on the chip-site lands;

applying an under fill resin around the chip-site lands and the first solder balls;

disposing a plurality of second solder balls on corresponding bonding pads disposed on a semiconductor chip;

aligning the first solder balls with corresponding second solder balls;

connecting the first and second solder balls by melting the first solder balls; and

hardening the underfill resin.

17. The method of claim 16, wherein the connecting the first and second solder balls includes disposing the substrate on an assembling stage before melting the first solder balls.

18. The method of claim 16, wherein the preparing the substrate prepares the substrate having the chip-site lands and a plurality of second chip-site lands, the

method further comprising:

disposing a plurality of third solder balls on the second chip-site lands;

applying a second underfill resin around the second chip-site lands ant the third solder balls;

disposing a plurality of fourth solder balls on corresponding bonding pads disposed on a second semiconductor chip;

aligning the third solder balls with corresponding fourth solder balls; and

hardening the second underfill resin.

19. The method of claim 16, further comprising:

disposing a plurality of external solder balls on corresponding external lands disposed on the second surface of the substrate after hardening the underfill resin; and

forming a plurality of internal solder joints from first and second solder balls by melting.

20. The method of claim 19, wherein the internal solder joints are formed at least one material selected from the group consisting of Sn-Bi, Sn-Bi-Ag, Sn-Zn, Sn-Zn-Bi, Sn-Bi-In, Bi-In, Sn-In, Bi-Pd, In-Ag, Sn-Ag, Sn-Ag-Cu, Sn-Pb, and Sn-Zn.

21. The method of claim 16, further comprising stacking a low dielectric constant film on the surface of the semiconductor chip, before disposing the second solder balls.

22. The method of claim 21, further comprising applying a protective film containing an organic synthetic resin on the surface of the semiconductor chip, after stacking the low dielectric constant film and before disposing the second solder balls.